DRAWINGS

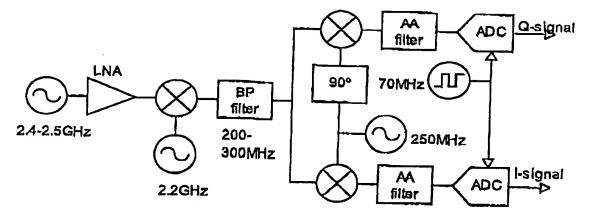


Figure 1

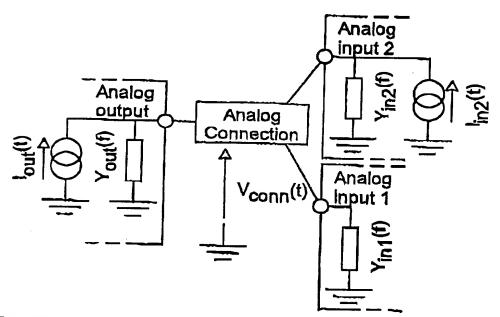
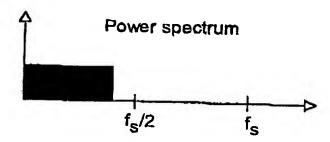


Figure 2



Equivalent low-pass representation

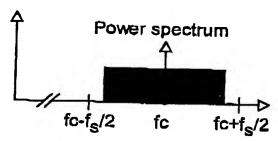


Figure 3

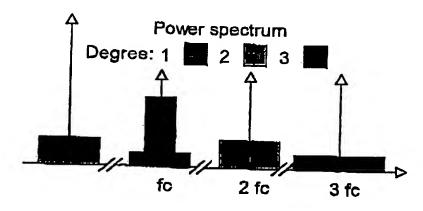


Figure 4

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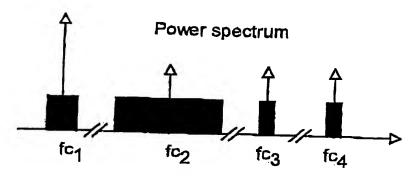
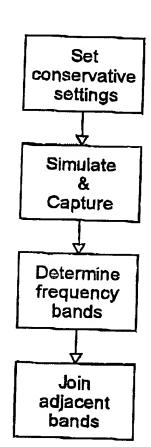


Figure 5



Pigure 6

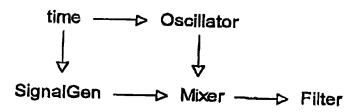


Figure 7

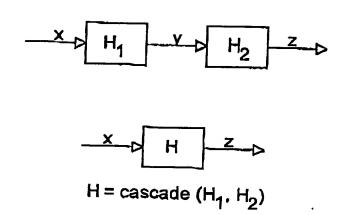
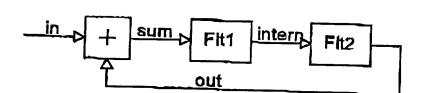


Figure 8



Pigure 9

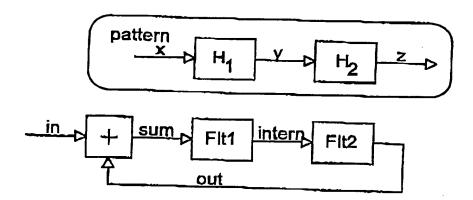


Figure 10

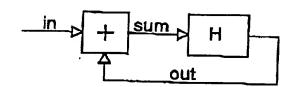


Figure 11

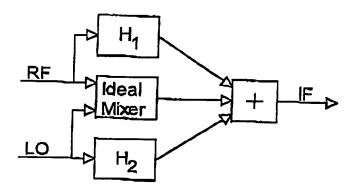


Figure 12

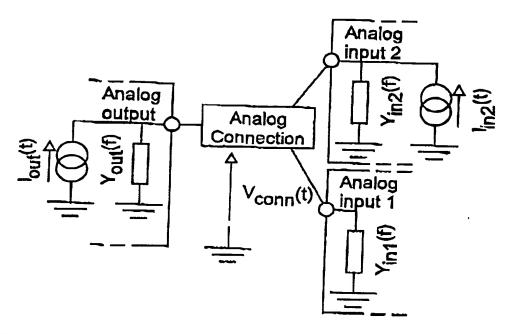


Figure 13

$$|_{\text{out}} \rightarrow |_{\text{conn}} \rightarrow |_{\text{lin2}} \rightarrow |_{\text{lin2}} \rightarrow |_{\text{H(f)}} \rightarrow |_{\text{conn}} \rightarrow |_{\text{lin2}} \rightarrow |$$

Figure 14

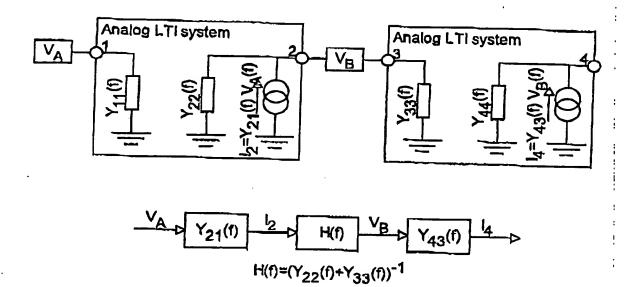


Figure 15

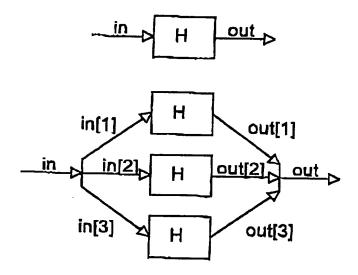
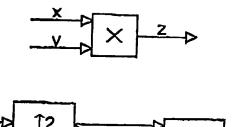


Figure 16



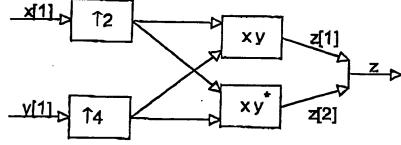


Figure 17

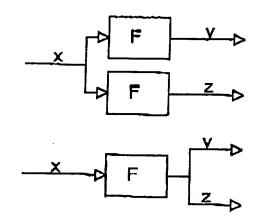


Figure 18

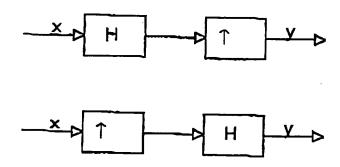


Figure 19

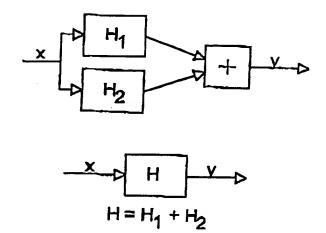


Figure 20

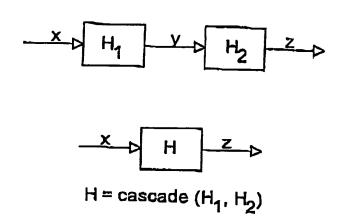


Figure 21

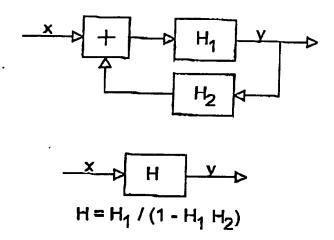


Figure 22

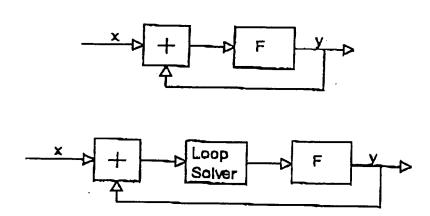
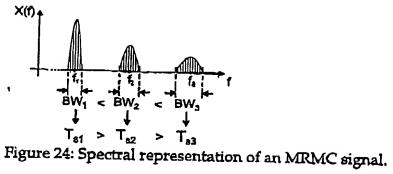


Figure 23



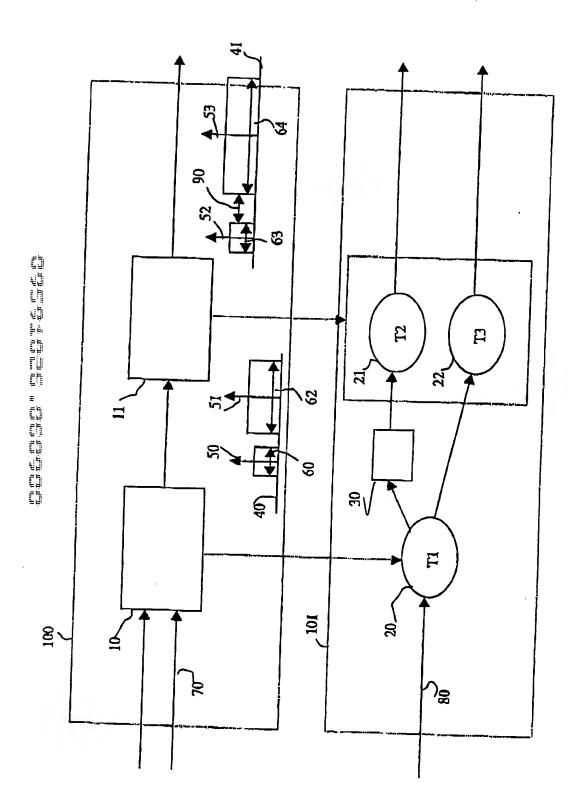


Figure 25

Preliminary Simulation signal representations Computational graph	in plurality of nodes Determine computation in plurality of nodes method for nonlinear circuits
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Scheduling of computation nodes - preferring vector processing modes

Executed Scheduled Computation Rules

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Banklin